INTEGRATED CIRCUIT MODIFICATION USING WELL IMPLANTS

Cross Reference to Related Applications

This application claims the benefits of US Provisional Patent Application No. 60/433,314 filed December 13, 2002, the disclosure of which is hereby incorporated herein by reference.

This application is also related to US Patent Application No. 09/758,792 and to US Patent Application No. 09/882,892 filed June 15, 2001 mentioned below.

Technical Field

The present invention relates to integrated circuits and semiconductor devices (ICs) in general and their methods of manufacture wherein the integrated circuits and semiconductor devices employ camouflaging techniques, which would make it difficult for the reverse engineer to discern how the semiconductor device is manufactured.

Related art

The present invention is related to the following US patents and patent applications by some of the same inventors as the present inventors:

(1) United States Patent Nos. 5,866,933 and 6,294,816 teach how transistors in a CMOS circuit are connected by implanted (and therefore hidden and buried) lines between the transistors by modifying the p+ and n+ source/drain masks. These implanted interconnections are used to make 3-input AND or OR circuits look substantially identical to the reverse engineer. Also, buried interconnects force the reverse engineer to examine the IC in greater depth to try to figure out the connectivity between transistors and hence their function.

(2) United States Patent Nos. 5,783,846; 5,930,663 and 6,064,110 teach a further modification in the source/drain implant masks so that the implanted connecting lines between transistors have a gap inserted, with approximately the length of the minimum feature size of the CMOS technology being used. If this gap is "filled" with one kind of implant, the line conducts; but if it is "filled" with another kind of implant, the line does not conduct. The intentional gaps are called "channel blocks." The reverse engineer is forced to determine connectivity based on resolving the implant type at the minimum feature size of the CMOS process being used.

(3) United States Patent No. 6,117,762 teaches method and apparatus for protecting semiconductor integrated circuits from reverse engineering. Semiconductor active areas are formed on a substrate and a silicide layer is formed both over at least one active area of the semiconductor active areas and over a selected substrate area for interconnecting the at least one active area with another area through the silicide area formed on the selected substrate area.

(4) United States Patent No. 4,583,011 discloses a method and circuit arrangement for foiling an attempt to copy a MOS integrated circuit by implementing in the circuit an additional pseudo MOS device, which from its location in the circuit would appear to a would-be copier to be an enhancement mode device. However, the pseudo MOS device is implemented with a depletion implant.

(5) United States Patent No. 5,973,375 discloses connections between implanted regions of adjacent transistors in a semiconductor substrate are made by buried conductive implants under field oxide layers. Buried conductive implants also referred to as buried contacts have doping concentrations similar to the doping concentrations of source/drain implants. Typical buried contacts have a doping concentration on the order of 10^{18} atoms/CM^3.

(6) United States Patent Application No. 09/758,792 discloses a double poly process technique that allows transistors to be ON or OFF depending upon implant details.

(7) United States Patent Application No. 09/882,892, filed on June 15, 2001 and a related PCT application PCT/US02/19075 filed on June 13, 2002, discloses a buried contact implant used under the gate region. The buried contact structure used in the patent application has approximately the same doping concentrations and depth of source/drain implants.

Background of the Invention

The creation of complex integrated circuits and semiconductor devices can be a very expensive undertaking given the large number of hours of sophisticated engineering talent involved in designing such devices. Additionally, integrated circuits can include read-only memories into which software, in the form of firmware, is encoded. Further, integrated circuits are often used in applications involving the encryption of information, and therefore in order to keep such information confidential, it can be desirable to keep such devices from being reverse engineered. Thus, there can be a variety of reasons for protecting integrated circuits and other semiconductor devices from being reversed engineered.

In order to keep the reverse engineer at bay, different techniques are known in the art to make integrated circuits more difficult to reverse engineer. One technique that is used is to make the connections between transistors difficult enough to determine that the reverse engineer must carefully analyze each transistor (in particular, each CMOS transistor pair for CMOS devices), and not use automatic circuit and pattern recognition techniques in order to reverse engineer the integrated circuit. Since integrated circuits can have hundreds of thousands or even millions of transistors, forcing the reverse engineer to carefully analyze each transistor in a device can effectively frustrate the reverse engineer's ability to reverse engineer the device successfully.

The prior art techniques mentioned above, if successful, will force the reverse engineer to study the metal connections to try to figure out the boundaries of standard circuits and to try to figure out their function. For example, gate connections may utilize the polysilicon layer (the first polysilicon layer in a process having two or more polysilicon layers) and the reverse engineer would look for these contacts, knowing that these gate contacts are typically the input to transistors and hence to a standard circuit. In addition, the source and drain contacts are made to the substrate via metal interconnects. One way in which the reverse engineer might work would be to look for cell boundaries by means of looking for silicon-to-gate poly metal lines, as these suggest the possibilities for contacts between the output (the drain contact) from one transistor cell into the input (the gate contact) of a next transistor cell. If this can be done, the reverse engineer can define cell boundaries by these silicon-gate poly lines. Then, by noting

the cell boundaries, the reverse engineer can find the cell characteristics (for example, size and number of transistors) and from this make reasonable assumptions as to the cell's function. In addition to cell boundaries, the reverse engineer may also rely upon the size of the transistor and its location. For example, P-channel devices (PMOS) are larger than N-channel devices (NMOS), and all PMOS devices are grouped in one row while all NMOS devices are grouped in a different row. This information could then be stored in a database for automatic classification of other similar cells.

It is an object of this invention to make reverse engineering more difficult and, in particular, to force the reverse engineer to study implants under the gates. It is believed that this will make the reverse engineer's efforts all the more difficult by making it very time consuming, and perhaps making it exceedingly impractical, if not impossible, to reverse engineer a chip employing the present invention. The present invention can be used harmoniously with techniques disclosed in the prior United States Patents and patent applications identified above to further confuse the reverse engineer.

Figure 1a depicts a simplified cross-section of a prior art single well CMOS device. In a NMOS device, shown on the left, an active region 16a is typically a n-type source region, while

active region 18a is typically a n-type drain region disposed in a p-type substrate 12. A gate 20a

may be manufactured out of a layer of polysilicon 19 disposed upon a layer of gate oxide 21. A

gate 20a is disposed between the two active regions 16a, 18a. Field Oxide 10 isolates the NMOS

device from the PMOS device of the CMOS pair and other semiconductor devices within the IC.

In a PMOS device, shown on the right, an active region 16b is typically a p-type source region,

while active region 18b is typically a p-type drain region disposed in a n-type well 42 of the

substrate 12. A gate 20b may be manufactured out of a layer of polysilicon 19 disposed upon a layer of

gate oxide 21. The gate 20b is disposed between the two p-type active regions 16b, 18b. The n-type well

42 isolates the p-type active regions 16b, 18b from the p-type substrate 12.

Figure 1b depicts a simplified cross-section of another prior art CMOS device. Two

major goals in the semiconductor industry are to increase the density and to increase the speed of

digital or analog integrated circuits (ICs). Increasing the density means using smaller channel

lengths and widths. In order to satisfy the conditions such as separation of highly integrated fine

or minute elements of a semiconductor device, some n-type devices of a CMOS pair having a

substrate of a first conductivity type have a well of the same conductivity type as the substrate.

Figure 1b is a simplified cross-sectional view of such a prior art CMOS device, the NMOS

device being shown on the left while the PMOS device is shown on the night. The NMOS device

has a well 14 of a first conductivity type formed in the first conductivity type semiconductor

substrate 12. In the example shown in Figure 1b, the substrate 12 is a p-type semiconductor

substrate and well 14 is a p-type well. The source region 16a and drain region 18a of the NMOS

device have a second conductivity and are preferably of n-type. Field Oxide 10 isolates the

NMOS device from the PMOS device in the CMOS pair and also isolates the semiconductor

device from other semiconductor devices within the IC. The gates 20a, 20b are manufactured

out of a layer of polysilicon 19 disposed on a layer of gate oxide 21. In the PMOS device, the

source region 16b and drain region 18b are p-type. Under the source region 16b and drain region

18b is a n-type well 42.

The present invention preferably makes use of a standard CMOS manufacturing process

called a "double well process" in which the semiconductor substrate of a first conductivity has a

well having a first conductivity type, and a well having a second conductivity type. One skilled

in the art will appreciate, after reading this patent, that the present invention may also make use of other CMOS processes that are not double well processes. Masks are used to determine the location and shapes of the first conductivity type wells and the second conductivity type wells.

As will be seen, changing the location of the different wells forms a conduction path between two active regions, such as the source and drain. Thus, the resulting semiconductor device will be permanently ON for any reasonable gate voltage. Therefore, with the present invention, the circuit may be constructed to look the same as some conventional circuits, but the functionality of selected transistors will be quite different and therefore the circuit will function quite differently from the circuit that it visually mimics. Since the reverse engineering process looks for repeating patterns of circuit devices (as seen from a top or plan view) and assumes that all repeating patterns reflect the same circuit functions, the reverse engineer is apt to assume an incorrect function when trying to copy the original integrated circuit. Thus, the real functionality of the integrated circuit in which the present invention is used is hidden. Of course, if this technique of making a pattern of transistors mimic a conventional circuit but perform a different function is used hundreds or thousands of times in a complex integrated circuit having perhaps millions of transistors, the reverse engineer ends up with not only a device which does not work, but also a daunting task of trying to figure out what went wrong with the assumptions that he or she made in analyzing the chip to be reverse engineered. This additional effort, if undertaken, forces the reverse engineer to spend additional time trying to determine how the chip in question is really configured.

The present invention not only provides a device and method that will confuse the reverse engineer, but it also provides a simpler path to implementation than other methods of inhibiting the reverse engineering process. The technique disclosed herein may be utilized to modify the library design of a particular vendor as opposed to forming a completely new and different appearing library. Thus, those skilled in the art will appreciate that the cost and time associated with the present invention is less than other methods used to inhibit integrated circuits from being reverse engineered.

Note that the present invention might only be used once in a thousand of instances of what appears to be a semiconductor device or a pattern of devices on the chip in question, but the

reverse engineer will have to look very carefully at each semiconductor device or pattern knowing full well that for each semiconductor device or pattern that he or she sees, there is a very low likelihood that it has been modified by the present invention. The reverse engineer will be faced with having to find the proverbial needle in a haystack.

Briefly, and in general terms, the present invention comprises a method of camouflaging an integrated circuit for the purpose of deterring a reverse engineer, wherein a well of the same type as the source and drain regions is placed under the gate region in contact with the source and drain region.

In another aspect, the present invention provides for camouflaging an integrated circuit structure. The integrated circuit structure is formed by a plurality of wells. The well under the gate region being disposed adjacent to the same type source and drain regions.

Description of the Drawings

Figure 1a is a simplified cross-sectional view of a prior art CMOS device with a single well process;

Figure 1b is a simplified cross-sectional view of a prior art CMOS device having a substrate of a conductivity type and a well of the same conductivity type for the n-type device made by a double-well process;

Figure 2 is a simplified cross-sectional view of a CMOS device depicting one embodiment of the present invention;

Figure 3 is a simplified cross-sectional view of a CMOS device in which the n-type device has been modified in accordance with the present invention;

Figures 4a through 4c are exemplary simplified process sequences for a single well CMOS device in accordance with the present invention;

Figures 5a through 5d are exemplary simplified process sequences for a double well CMOS device in accordance with the present invention;

Figures 6a through 6d are a second set of exemplary simplified process sequences in accordance with the present invention;

Figure 7 is an exemplary simplified cross-sectional view of a CMOS device in which the p-type device has been modified in accordance with the present invention; and

Figure 8 is another exemplary simplified cross-sectional view of a CMOS device in which the p-type device has been modified in accordance with the present invention.

Detailed Description

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which the preferred embodiments of the invention are shown. This invention may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

Figure 2 shows how the NMOS and PMOS devices within the CMOS of Figure 1b can be intentionally turned ON by the present invention to give the appearance of a functioning transistor device to the reverse engineer when in fact the transistor is never turned OFF.

As shown in Figure 2, p-type well 14 of Figure 1b has been replaced by n-type well 7 and n-type well 42 of Figure 1b has been replaced by p-type well 8. One skilled in the art will appreciate that changing the type of wells requires changing the openings in the masks during the formation of the p-type and n-type wells 7, 8. By changing the wells such that a n-type well 7 is between the n-type active regions 16a, 18a an electrical path is formed between active region 16a and active region 18a regardless of the voltages applied. The result is a transistor that is always ON, regardless of any reasonable voltage applied to the gate 20a. Further, by changing the wells such that a p-type well 8 is between the p-type active regions 16b, 18b an electrical path is formed between active region 16b and active region 18b regardless of the voltages applied. The result is a transistor that is always ON, regardless of any reasonable voltage applied to the gate 20b. A reasonable voltage refers to any gate voltage found in normal device operation such that the voltage does not break down the gate oxide 21.

Figure 3 illustrates a simplified cross section of a CMOS device in accordance with another embodiment of the present invention. One skilled in the art will appreciate that the NMOS device of the CMOS pair of Figure 1b may be modified without modifying the PMOS device of the CMOS pair. Thus, in Figure 3, the p-type well 14 of Figure 1b is replaced by the n-type well 7, while the PMOS device on the right remains unchanged from Figure 1b to Figure 3.

While the devices of Figures 2 and 3 provide devices that are always ON, the devices also pose leakage problems. If not all devices in a circuit are modified, then wells 7, 8 under the gate regions 20a, 20b which are the same conductivity type as the source and drain regions 16a, 18a, 16b, 18b may cause a current leakage if they are in close enough contact to each other. For example, in Figure 3, it is possible that current from n-type well 7 could leak into n-type well 42 causing problems with the PMOS transistor of Figure 3. Thus, if such leakage current is a problem, it is preferred that the wells 7, 8 be made smaller than the transistor to avoid this type of leakage. Thus the devices shown in Figures 4a - 8 depict wells under the gate regions that are smaller than the associated transistors. While one skilled in the art will appreciate that this is not

9

necessary, it does prevent the invention from causing other leakage problems within the circuit should that be of concern.

Figures 4a-4c show how the semiconductor device depicted in Figure 1a can be intentionally turned ON by the present invention to give the appearance of a functioning transistor device to the reverse engineer when in fact the transistor is never tamed OFF. The processing steps preferably utilized to arrive at the device shown in Figure 4c will be discussed subsequently.

The CMOS transistor pair in Figure 4c comprises a NMOS device, shown on the left and a PMOS device shown on the right. The NMOS transistor in Figure 4c has a p-type substrate 12, two n-type active regions 16a, 18a and a gate 20a. The PMOS field-effect transistor in Figure 4c has a p-type substrate 12, a n-type well 42, two p-type active regions 16b, 18b and gate 20b. The two n-type active regions 16a, 18a are typically referred to as source and drain regions. While this terminology may lose its meaning with respect to the present device, which is always ON, the use of the terms source and drain will be maintained for ease of understanding and comparison with conventional circuits. Beneath the gate 20a is an additional n-type well 22 connecting active regions 16a, 18a. The additional well 22 is the same conductivity type as the active regions 16a, 18a, thereby providing a conduction path between the active regions 16a, 18a regardless of the voltages applied. The result is a transistor that is always ON, regardless of any reasonable voltage applied to the gate 20a. A reasonable voltage refers to any gate voltage found in normal device operation such that the voltage does not break down the gate oxide 21. One skilled in the art will appreciate that the sizes of the features of the device shown in Figure 4c, when viewed in a conventional plan view, would lead the reverse engineer to believe that this device is a normal NMOS device.

Prior art devices, such as those described in US Patent No. 5,973,375 and US Application No. 09/882,892 previously discussed, utilize buried contacts to connect active regions. One

skilled in the art will appreciate that the doping concentration of a source or drain implant is typically on the order of 10^{19} atoms/cm^3. The doping concentration of a well is typically on the order of 10^{13} atoms/cm^3 to 10^{15} atoms/cm^3. The doping concentration of a buried contact is typically on the order of 10^{18} atomscm^3. Thus, buried contacts refer to implants with a higher doping concentration than a well, typically much closer to the doping concentration of a source/drain implant. In the present device and method it is a well that is being used to provide the connection between the active regions. Further, the depth of a buried contact is generally more similar to the depth of the source/drain implants, while a well implant is generally deeper than the source/drain implants. Also, well 22 can be easily formed at the same time as well 42 is formed.

One skilled in the art will appreciate that there are a variety of different processes available for the manufacture of semiconductor devices. The following discussion is provided as an example relating to a 0.35 μm process in accordance with the present invention. The present invention may also be applied to other processes using the same basic methodology, although the exact details, such as dimensions and doping levels, will differ. Process steps used to make the devices shown in Figures 1a and 1b are well known in the art of manufacture of semiconductor devices; therefore, conventional processing steps are not discussed in any detail. Rather, the following simplified explanation is provided to elaborate on the process steps and process features preferably used to practice the present invention in terms of how the process steps differ from conventional process steps.

Figures 4a-4c depict processes that may be used in forming a device in accordance with the present invention. Turning to Figure 4a, a resist mask 36 is formed on a substrate 12 of a NMOS transistor. The substrate 12 is made of, for example, p-type silicon having a resistivity of, for example, 10 Ω/cm. In conventional processing, the resist mask 36 is etched and removed only over the PMOS transistors. In the present process, the resist mask is preferably etched to form an opening 35 over a portion of the NMOS transistor. The width 26 of the opening 35 is preferably greater than or equal to the minimum n-well width

11

for the given process. For a 0.35 µm process, the minimum n-well width is typically 0.6 µm. Phosphorous ions 34 are preferably implanted into the substrate 12 so as to form a phosphorous implanted region, herein referred to as n-well 22 for the NMOS device and n-well 42 for the PMOS device, shown in Figure 4b. The phosphorous ions 34 may be implanted, for example, at an acceleration voltage of 180 keV and a dose of about 5.0×10^{13} CM^{-2}. The implantation of the phosphorous ions results in a n-well 22 located beneath the gate region 20 of Figure 4b, and a n-well 42 located beneath the PMOS device. Typically, after the implantation of the phosphorus ions the substrate is preferably temperature cycled to drive in the ions to the desired depth in the substrate.

In Figure 4b, the resist mask 36 has been removed and a gate oxide layer 21 and polysilicon layer 19 are formed over the surface of the substrate 12. For the NMOS device, a gate 20a is formed on the substrate 12 preferably by etching the gate oxide layer 21 and polysilicion layer 19. Phosphorous ions 38 may then be implanted, for example, into the substrate 12, to form n-regions 16a, 18a as shown in Figure 4c. The phosphorous ions 38 may be implanted, for example, at an acceleration voltage of 20 keV and a dose of 5.0×10^{15} CM^{-2}. One skilled in the art will appreciate that the concentration of phosphorous ions 38 is much larger when the n-regions 16a, 18a are formed compared to the concentration of phosphorous ions 34 when the n-wells 22, 42 are formed. One skilled in the art will appreciate that the combination of temperature and ion concentration can be varied in accordance with typical semiconductor process such that the desired depth of the various implants can be obtained. Preferably, the temperature cycles and the ion concentrations are chosen such that the n-type wells 22, 42 are deeper than the n-type source and drain regions 16a, 18a. The PMOS device shown in Figures 4a-4c is formed according to conventional process steps.

Figures 5a-5d depict an exemplary set of process steps that may be used in producing a double well CMOS device in accordance with the present invention. Turning to Figure 5a, a resist mask 36 is formed on a p-type substrate 12 of a NMOS transistor. In a standard double

well semiconductor process, the resist mask 36 would cover the entire NMOS transistor region, and only the areas of the PMOS transistor region would be uncovered. The resist mask 36 is preferably etched over a portion of the NMOS transistor for forming an opening 35. The substrate 12 is made of, for example, p-type silicon having a resistivity of preferably 10 Ω/cm. Phosphorous ions 34 are implanted into the substrate 12 to form a phosphorous implanted region, herein referred to as n-wells 22, 42, shown in Figure 5b. The phosphorous ions 34 may be implanted, for example, at an acceleration voltage of 180 keV and a dose of about 5 x 10^{13} CM^{-2}. The implantation of the phosphorous ions results in an n-well 22 located beneath the gate region of the NMOS device, and in a n-well 42 located beneath the PMOS device. The width 26 of the opening 35 is preferably greater than or equal to the minimum n-well width for the given process. For a 0.35 μm process, the minimum n-well width is typically 0.6 μm. The substrate is preferably temperature cycled to drive in the ions to the desired depth.

In Figure 5b, the resist mask 36 has been removed and another resist mask 32 is formed on the substrate 12. In the present embodiment, the resist mask 32 is preferably etched to form two openings 33, 37, such that the portion of the resist mask 32 extends a distance 24 past the edge of the n-well 22. For the 0.35 μm process the distance 24 is typically equal to 0. 16 μm, i.e. the minimum n-well to p-well separation. Boron ions 30 are implanted into the substrate 12 to form boron-implanted regions, herein referred to as p-wells 14a, 14b, shown in Figure 5c. The boron ions 3 0 may be implanted, for example, at an acceleration voltage of 100 keV and a dose of about 3 x 10^{13} CM^{-2}. In prior art processes, the resist mask 32 over n-well 22 would not be present, thus the prior art p-well 14 extends under the gate region 20a as shown in Figure lb. The resist mask 32 over n-well 22 allows for control of the implantation of the region under the gate 20a. This boron region 14a, 14b is actually the p-well implant in a twin well process. As before, the substrate is typically temperature cycled to drive in the ions to the desired depth.

In Figure 5c, the resist mask 32 has been removed and a gate oxide layer 21 and a polysilicon layer 19 is formed on the substrate 12. For the NMOS device, the gate oxide layer 21

and the polysilicon layer 19 are preferably etched to form the gate 20a. For the PMOS device, the gate

oxide layer 21 and the polysilicon layer 19 form a resist mask over the PMOS device. Phosphorous ions

38 may be implanted, for example, into the substrate 12, to form n-type active regions 16a, 18a as shown

in Figure 5d. The phosphorous ions 38 may be implanted, for example, at an acceleration voltage of 70 keV

and a dose of 5 x 10^{15} cm^{-2}. One skilled in the art will appreciate that the concentration of phosphorous

ions 38 is much larger when the active regions 16a, 18a are formed compared to the concentration of

phosphorous ions 34 when the n-wells 22, 42 are formed. One skilled in the art will appreciate that the

combination of temperature and ion concentration may be varied in accordance with typical semiconductor

process such that the desired depth of each region can be obtained. Preferably, the temperature

cycles and the ion concentrations are chosen such that the n-type wells 22, 42 are deeper than the

n-type source and drain regions 16a, 18a. In addition, in some applications the temperature

cycles and ion concentrations are preferably chosen such that the n-type wells 22, 42 are deeper

than the p-type wells 14a, 14b.

There are other methods, other than the manufacturing process described above and

shown in Figures 5a-5d, which may be used to provide the device shown in Figure 5d. A second

method is shown in Figures 6a-6d. In Figure 6a, the first step is the same as the step shown in

Figure 5a.

In Figure 6b, however, the process step is different than the step shown in Figure 5b. In

Figure 6b, the resist mask 32 is not placed over the n-type well 22 of the NMOS device. Boron

ions 30 are implanted into the substrate 12 so as to form a boron implanted region, herein

referred to as p-well 14, shown in Figure 6c. The boron ions 30 may be implanted, for example,

at an acceleration voltage of 100 keV and a dose of about 3 x 10^{13} CM^{-2}. One skilled in the art

will recognize that the p-well 14 is being implanted over the n-well 22, therefore the density of

the phosphorous ions 34 forming the n-well 22 must be greater than the density of the boron ions

30 forming the p-well 14. Thus, the region under the gate 20a remains n-type due to the presence of n-well 22.

In Figure 6c, the resist mask 32 has been removed and a gate oxide layer 21 and a polysilicon layer 19 is formed on the substrate 12. For the NMOS device, the gate oxide layer 21 and the polysilicon layer 19 are preferably etched to form the gate 20a. For the PMOS device, the gate oxide layer 21 and the polysilicon layer 19 form a resist mask over the PMOS device. Phosphorous ions 38 may be implanted, for example, into the substrate 12 to form n-type active regions 16a, 18a as shown in Figure 6d. The phosphorous ions 38 may be implanted, for example, at an acceleration voltage of 20 keV and a dose of 5×10^{15} cm^{-2}. One skilled in the art will appreciate that the concentration of phosphorous ions 38 is much larger when the active regions 16a, 18a are formed compared to the concentration of phosphorous ions 34 when the n-wells 22, 42 are formed. One skilled in the art will appreciate that the combination of temperature and ion concentration can be varied in accordance with typical semiconductor process such that the desired region/well depth can be obtained. Preferably, the temperature cycles and the ion concentrations are chosen such that the n-type wells 22, 42 are deeper than the n-type source and drain regions 16a, 18a. In addition in some applications, the temperature cycles and ion concentrations are preferably chosen such that the n-type wells 22, 42 are deeper than the p-type well 14. This insures that n-type well 22 overrides p-type well 14.

One skilled in the art will appreciate that the p-type wells 14a, 14b are not required in order for the device to be always ON. However, given the small feature size of conventional devices, it is common for the devices to have a p-type well 14 of the same conductivity type as the substrate 12, as shown in Figure 1b. In the preferred embodiment, the techniques described herein are used in standard twin-well CMOS manufacturing processes and as such, p-type wells 14a, 14b are used to avoid unnecessary modification of the semiconductor manufacturing process. In addition, the p-type wells 14a, 14b enable the NMOS device to withstand higher applied voltages. Further, the p-type wells 14a, 14b help to insulate that n-type active regions

15

]6a:, 18a from the substrate 12. However, one skilled in the art will appreciate that the semiconductor

manufacturing process may be modified such that the p-type wells 14a, 14b are not provided in the device,

as shown in Figures 4a-4c.

Another embodiment of the present invention utilizes a permanently ON PMOS

transistor. Without adding additional processing steps to the formation of the semiconductor

device, the PMOS device formed by the present invention can always be ON but shorted to the

substrate. In the prior art PMOS transistors, such as the one shown in Figure 1b, the n-well 42 is

implanted first. Next, p-regions 16b, 18b are implanted to form the source and drain of the

PMOS transistor.

Figure 7 depicts a cross-section of a CMOS device, where the PMOS transistor on the

right has been modified in accordance with the present invention. The concept and process is

similar to the process involving the NMOS transistor. However, a p-well 52' is implanted in the

substrate 12 under the gate region 20b. It is possible that a dosage of boron ions used to create

the p-well 52' is enough in the standard process to overcome the implanted n-well 42 at the

surface of the substrate 12. Thus, the conduction path will be present from source and drain p-

regions 16b, 18b through the channel 52' to the p-type substrate 12. Therefore, the

semiconductor device will always be ON for a reasonable gate voltage, but also shorted to the

substrate 12.

One skilled in the art will appreciate that in some applications it may be

undesirable for the semiconductor device to be shorted to the substrate as shown in Figure 7.

Figure 8 depicts a cross-sectional view of a CMOS device, where the PMOS transistor on the

right has been modified in accordance with the present invention, where the PMOS device is not

shorted to the substrate 12. The concept and process is similar to the process involving the

PMOS transistor described above with reference to Figure 7. However, a p-well 52" is

implanted in the substrate 12 under the gate region 20b. The dosage of boron ions used to create

16

the p-well 52" is enough to overcome the n-type well 42 at the surface of the substrate between the active regions 16b, 18b. However, the depth of p-type well 52" is controlled to be slightly shallower than n-type well 42. Thus, n-type well 42 prevents p-type well 52" from shorting to the substrate 12. One skilled in the art will appreciate that the process may already have processing steps which result in the n-well 42 being deeper than the p-well 52" while p-well 52" overrides n-well 42 at the surface of the substrate. In this case, the processes would not require modification.

In Figure 7, p-well 52' is deeper than and overrides n-well 42. Thus, any voltage applied to either p-type region 16b, 18b will pass to p-well 52' and short to p-type substrate 12. In Figure 7, one skilled in the art will appreciate that n-well 42 is optional because it does not change the operation of the circuit. If the device shown in Figure 6d is being manufactured with the same processes as the device of Figures 7 or 8 and the manufacturer desires to place the p-type well 14 of Figure 6d, or the n-type well 42 of Figure 7 to further confuse the reverse engineer, then an extra processing step would be required to ensure p-well 52', 52" overrides n-well 42 at the surface of the substrate 12. In Figure 6d, it is important for the operation of the false transistor that the n-well 22 override the p-well 14 at the surface of the substrate 12. However, in the Figures 7 and 8 it is important that the p-well 52', 52" override the n-well 42 at the surface of the substrate 12 in order to provide an electrical path between active regions 16b, 18b. Thus, in order to form both a PMOS and NMOS device in accordance with the present invention, two different p-well steps are required. Each p-well step will have a slightly different density of boron ions and/or different temperature cycles to ensure that in one step p-well 52' of Figure 7 or p-well 52" of Figure 8 overrides n-well 42, while in the other step p-well 14 of Figure 6d does not override n-well 22. Of course, one skilled in the art will appreciate that instead of using two different p-well process steps; two different n-well process steps could be used to achieve the same result.

If a PMOS and a NMOS device are both to be manufactured using a standard double-well manufacturing process without adding additional process steps, then one skilled in the art will appreciate that n-well 42 is generally not placed to ensure p-well 52 will be placed under gate region 20b. However, the structures shown in Figures 7 and 8 may be accomplished during double-well manufacturing processes. The manufacturing of the structures shown in Figures 7 and 8 may or may not require additional manufacturing steps depending upon the concentration profile of the n-wells and p-wells after implementation and temperature cycling.

It is very difficult for the reverse engineer to detect the techniques disclosed herein. For example, even when using microscopic investigates like SEM analysis on the top (plan view) side of the circuit of semiconductor devices altered by the techniques herein disclosed, the altered circuit will look identical to other standard semiconductor devices. Should the reverse engineer determine that further analysis of all millions of the semiconductor devices is required, then the metal, oxide, and insulation layers must be carefully removed. Next, the reverse engineer must perform a stain and etch to determine that the well implant has been placed where the gate had been. This will be difficult because for many dense ICs there will always be a well implant under the gate, only the well implant is usually a different type than the active regions adjacent to the gate region. However, in the case of the present invention, the well will be the same type as the semiconductor active regions adjacent to the gate region. Therefore, the reverse engineer must be able to determine between the different types of well conductivity types. Using the present techniques, the gate well implants are low dose. Thus, the chemical etches dependent on the chemical nature of the implanted material will not be as effective. As a result, it is believed that the techniques which will be needed to detect the use of the present invention will be sufficiently time consuming to deter the reverse engineer. A complex integrated circuit may comprise millions of semiconductor devices, and if the reverse engineer must carefully analyze each semiconductor device in order to determine whether or not the present invention has been used to disguise each semiconductor device, the effort involved in reverse engineering such an integrated circuit will be tremendous.

Having described the invention in connection with certain embodiments thereof, modification will now certainly suggest itself to those skilled in the art, for example, other doses or other types of semiconductor devices. As such, the invention is not to be limited to the disclosed embodiments, except as is specifically required by the appended claims.